VND5E050MJ-E
VND5E050MK-E

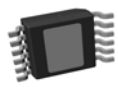
Double-channel high-side driver with analog current sense for automotive applications

Features

Max transient supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 V to 28 V
Max on-state resistance(per ch.)	R_{ON}	50 mΩ
Current limitation (typ)	I_{LIMH}	27 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected.

- General
  - Inrush current active management by power limitation
  - Very low standby current
  - 3.0 V CMOS compatible inputs
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - In compliance with the 2002/95/EC european directive
  - Very low current sense leakage
- Diagnostic functions
  - Proportional load current sense
  - High-precision current sense for wide currents range
  - Current sense disable
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Overtemperature shutdown with auto restart (thermal shutdown)
  - Reverse battery protected (see *Figure 29*)



PowerSSO-12



PowerSSO-24

  - Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VND5E050MJ-E and VND5E050MK-E are double-channel high-side drivers manufactured in the ST proprietary VIPower™ M0-5 technology and housed in the tiny PowerSSO-12 and PowerSSO-24 packages. The VND5E050MJ-E and VND5E050MK-E are designed to drive 12 V automotive grounded loads delivering protection, diagnostics and easy 3 V and 5 V CMOS compatible interface with any microcontroller.

The devices integrate advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel in order to provide enhanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication and overtemperature indication.

The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS_DIS pin high to allow sharing of the external sense resistor with other similar devices.

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Block diagram

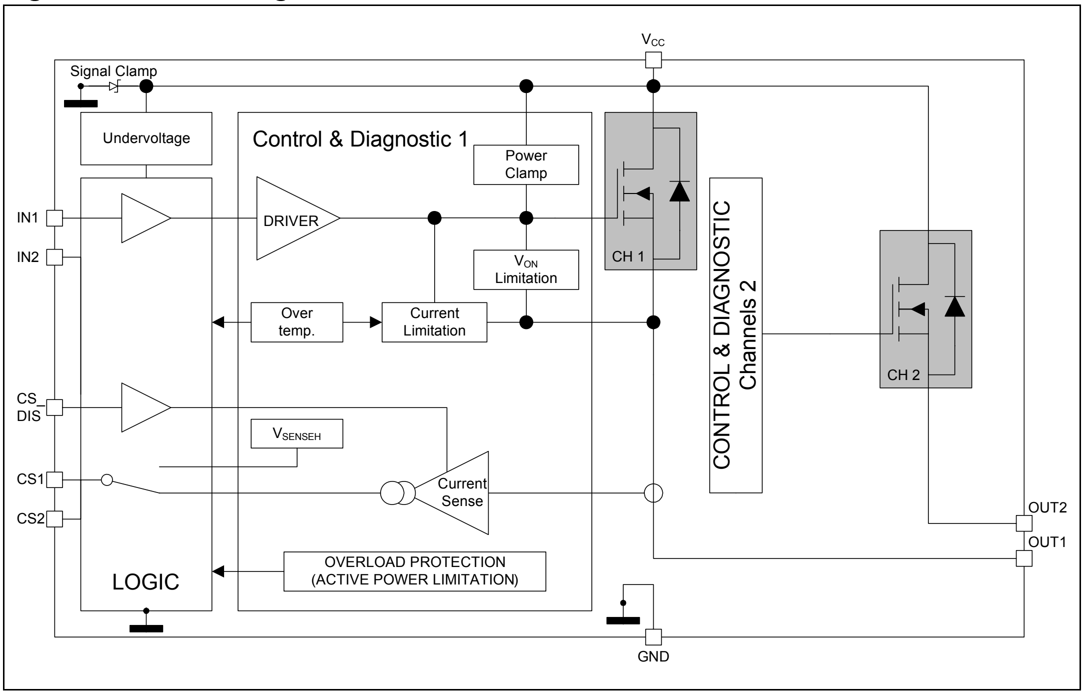


Table 1. Pin function

Name	Function
V_{CC}	Battery connection.
$OUT_{1,2}$	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
$IN_{1,2}$	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
$CS_{1,2}$	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

Figure 2. Configuration diagram (top view)

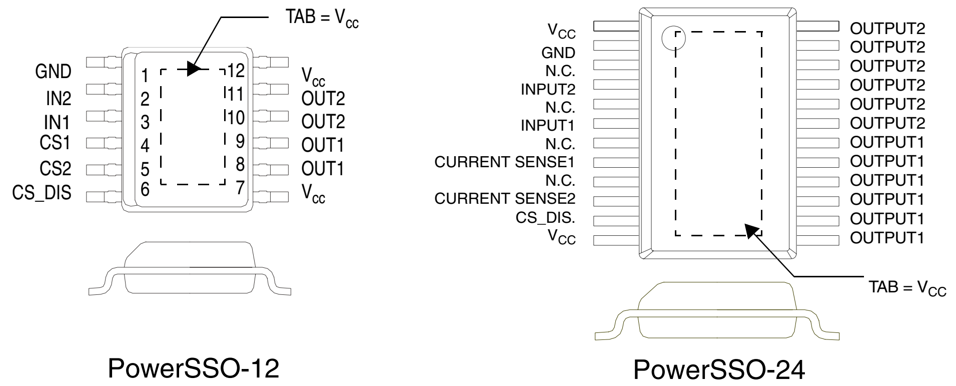
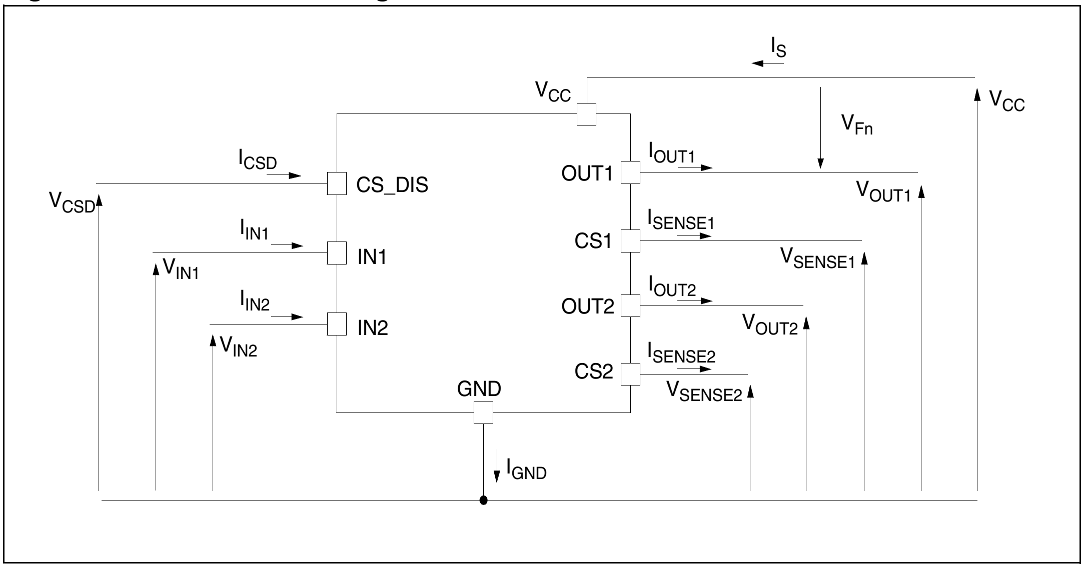


Table 2. Suggested connections for unused and not connected pins

Connection / pin	Current sense	N.C.	Output	Input	CS_DIS
Floating	Not allowed	X	X	X	X
To ground	Through 1 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions(1)



1. $V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	0.3	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	20	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
$-I_{CSENSE}$	DC reverse CS pin current	200	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 41 to +V_{CC}	V

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
E_{MAX}	Maximum switching energy (single pulse) ($L = 3$ mH, $R_L = 0\ \Omega$, $V_{bat} = 13.5$ V, $T_{jstart} = 150$ °C, $I_{OUT} = I_{limL}$ *(Typ.)*)	104	mJ
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ, C = 100 pF) - IN - CS - CS_DIS - OUT - V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	- 40 to 150	°C
T_{stg}	Storage temperature	- 55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value		Unit
		PowerSSO-12	PowerSSO-24	
$R_{thj\text{-}case}$	Thermal resistance junction-case (with one channel on)	2.7	2.7	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	See *Figure 33*	See *Figure 37*	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 28 V, -40 °C < T_j < 150 °C, unless otherwise stated.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	ON-state resistance(1)	I_{OUT} = 2 A, T_j = 25 °C			50	mΩ
		I_{OUT} = 2 A, T_j = 150 °C			100	
		I_{OUT} = 2 A, V_{CC} = 5 V, T_j = 25 °C			65	
V_{clamp}(2)	Clamp voltage	I_S = 20 mA	41	46	52	V
I_S	Supply current	OFF-state: V_{CC} = 13 V, T_j = 25 °C, V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} = 0 V		2(3)	5(3)	µA
		ON-state: V_{CC} = 13 V, V_{IN} = 5 V, I_{OUT} = 0 A		3	6	mA
$I_{L(off1)}$(2)	OFF-state output current (1)	V_{IN} = V_{OUT} = 0 V, V_{CC} = 13 V, T_j = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V, V_{CC} = 13 V, T_j = 125 °C	0		5	
V_F	Output-V_{CC} diode voltage(1)	-I_{OUT} = 4 A, T_j = 150 °C			0.7	V

1. For each channel.
2. Special characteristic according to ISO/TS 16949.
3. PowerMOS leakage included.

Table 6. Switching (V_{CC} = 13 V, T_j = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 6.5 Ω (see *Figure 5*)		20		µs
$t_{d(off)}$	Turn-off delay time	R_L = 6.5 Ω (see *Figure 5*)		45		µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 6.5 Ω		See *Figure 23*		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 6.5 Ω		See *Figure 25*		V/µs

Table 6. Switching (V_{CC} = 13 V, T_j = 25 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
W_{ON}	Switching energy losses during t_{won}	R_L = 6.5 Ω (see *Figure 5*)		0.15		mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 6.5 Ω (see *Figure 5*)		0.3		mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Hysteresis input voltage		0.25			V
V_{ICL}	Input voltage clamp	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
V_{CSDL}	Low-level CS_DIS voltage				0.9	V
I_{CSDL}	Low-level CS_DIS current	V_{CSD} = 0.9 V	1			µA
V_{CSDH}	High-level CS_DIS voltage		2.1			V
I_{CSDH}	High-level CS_DIS current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS voltage clamps	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		

Table 8. Protections and diagnostics (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short circuit current	V_{CC} = 13 V 5 V < V_{CC} < 28 V	19	27	38 38	A A
I_{limL}	Short circuit current during thermal cycling	V_{CC} = 13 V, $T_R < T_j < T_{TSD}$		7		A
T_{TSD}(2)	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C

Table 8. Protections and diagnostics (1) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DEMAG} (2)	Turn-off output voltage clamp	I_{OUT} = 2 A, V_{IN} = 0, L = 6 mH	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.1 A, T_j = -40 °C to +150 °C (see *Figure 7*)		25		mV

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.
2. Special characteristic according to ISO/TS 16949.

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.05 A, V_{SENSE} = 0.5 V, V_{CSD} = 0 V, T_j = -40 °C to 150 °C	1440	2250	3630	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1 A, V_{SENSE} = 4 V, V_{CSD} = 0 V, T_j = -40 °C to 150 °C T_j= 25°C...150°C	 1740 1750	 2070 2070	 2820 2562	
dK_1/K_1 (1)	Current sense ratio drift	I_{OUT} = 1 A, V_{SENSE} = 4 V, V_{CSD} = 0 V, T_j = -40 °C to 150 °C	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 2 A, V_{SENSE} = 4 V, V_{CSD} = 0 V, T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	 1900 1899	 2000 2000	 2395 2282	
dK_2/K_2 (1)	Current sense ratio drift	I_{OUT} = 2 A; V_{SENSE} = 4 V, V_{CSD} = 0 V, T_j = -40 °C to 150 °C	-9		9	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 4 A, V_{SENSE} = 4 V, V_{CSD} = 0 V, T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	 1969 1950	 1990 1990	 2210 2153	
dK_3/K_3 (1)	Current sense ratio drift	I_{OUT} = 4 A, V_{SENSE} = 4 V, V_{CSD} = 0 V, T_j = -40 °C to 150 °C	-6		6	%
I_{SENSE0} (2)	Analog sense leakage current	I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{CSD} = 5 V, V_{IN} = 0 V, T_j = -40 °C to 150 °C	0		1	µA
		I_{OUT} = 0 A, V_{SENSE} = 0 V, V_{CSD} = 0 V, V_{IN} = 5 V, T_j = -40 °C to 150 °C	0		2	
		I_{OUT} = 2 A, V_{SENSE} = 0 V, V_{CSD} = 5 V, V_{IN} = 5 V, T_j = -40 °C to 150 °C	0		1	
I_{OL}	Open load on-state current detection threshold	V_{IN} = 5 V, 8 V < V_{CC} < 18 V I_{SENSE} = 5 µA	4		20	mA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 4 A, V_{CSD} = 0 V	5			V

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSEH}	Analog sense output voltage in fault condition(3)	V_{CC} = 13 V, R_{SENSE} = 3.9 KΩ		8		V
I_{SENSEH}	Analog sense output current in fault condition(3)	V_{CC} = 13 V, V_{SENSE} = 5 V		9		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 4 A I_{SENSE} = 90% of $I_{SENSE\ max}$ (see *Figure 4*)		40	100	µs
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 4 A I_{SENSE} = 10% of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of INPUT pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 4 A I_{SENSE} = 90% of $I_{SENSE\ max}$ (see *Figure 4*)		80	250	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V, I_{SENSE} = 90% of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX} I_{OUTMAX} = 2 A (see *Figure 6*)			40	µs
$t_{DSENSE2L}$	Delay response time from falling edge of INPUT pin	V_{SENSE} < 4 V, 0.5 A < I_{OUT} < 4 A I_{SENSE} = 10% of $I_{SENSE\ max}$ (see *Figure 4*)		80	250	µs

1. Parameter guaranteed by design; it is not tested.
2. Special characteristic according to ISO/TS 16949.
3. Fault condition includes: power limitation and overtemperature.

Figure 4. Current sense delay characteristics

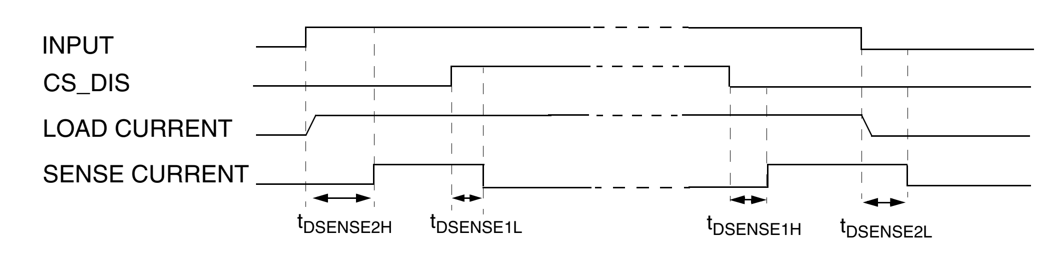


Figure 5. Switching characteristics

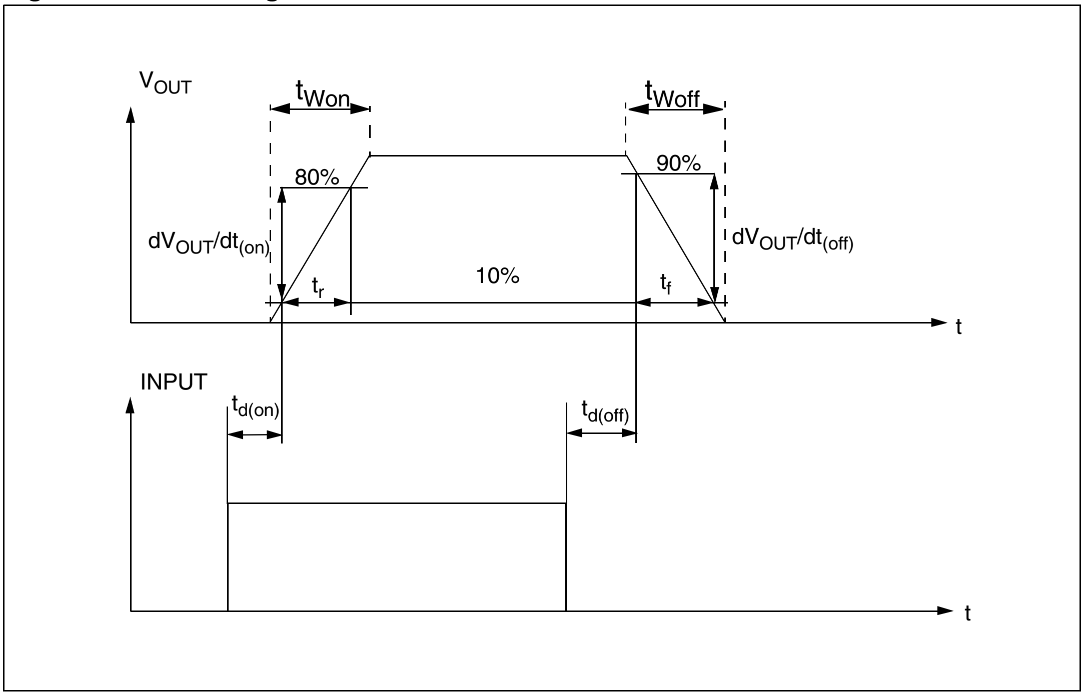
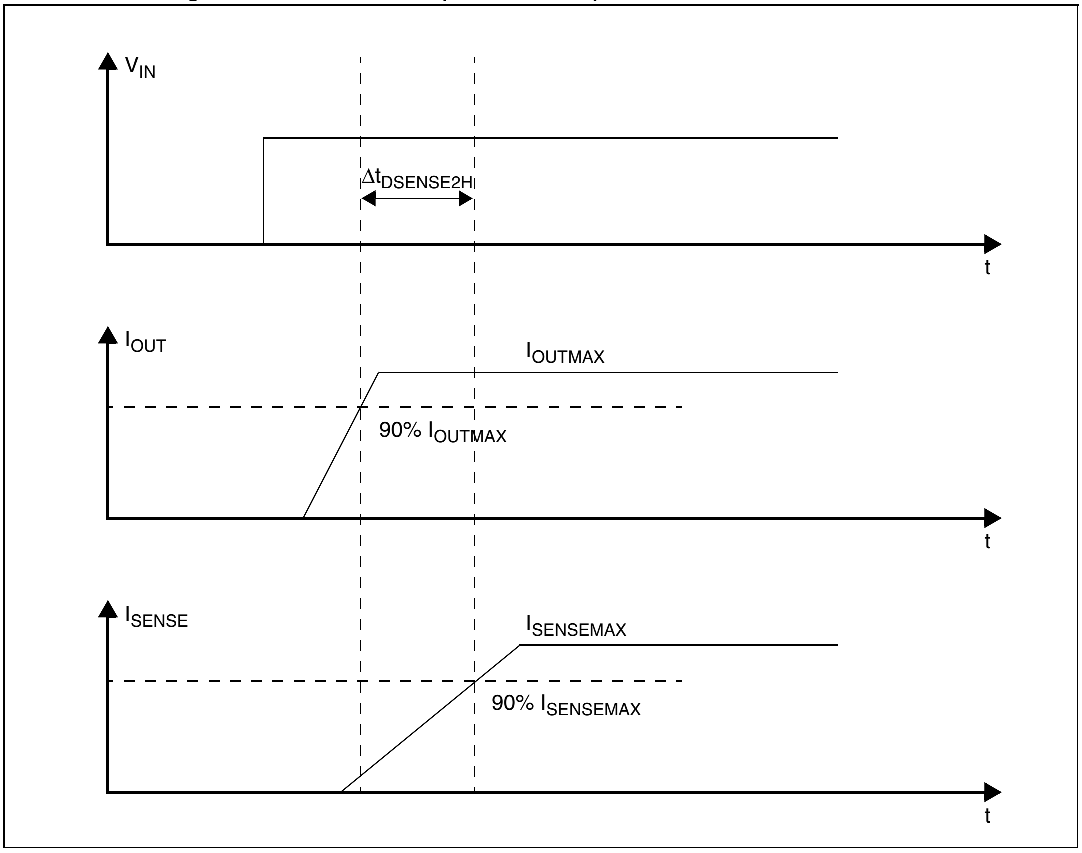


Figure 6. Delay response time between rising edge of output current and rising edge of current sense (CS enabled)



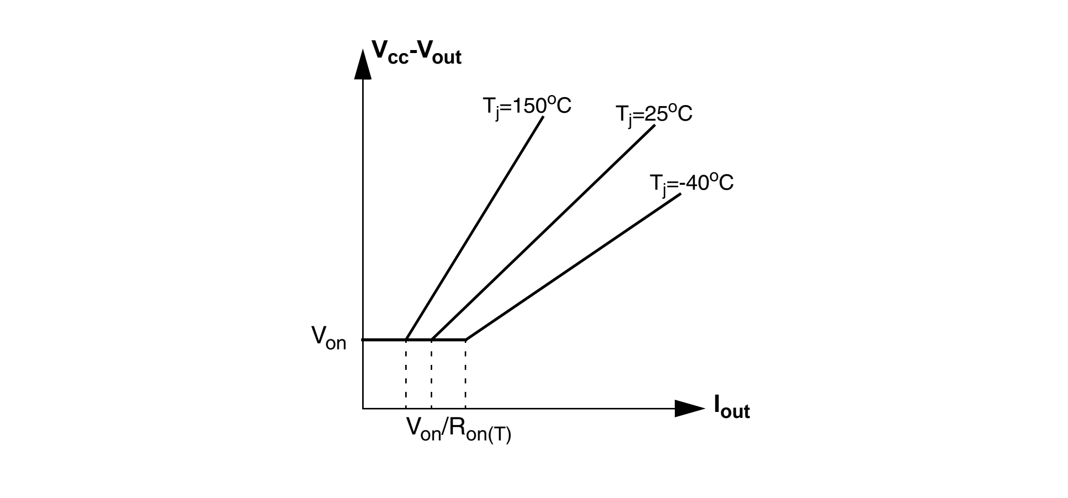


Figure 7. Output voltage drop limitation

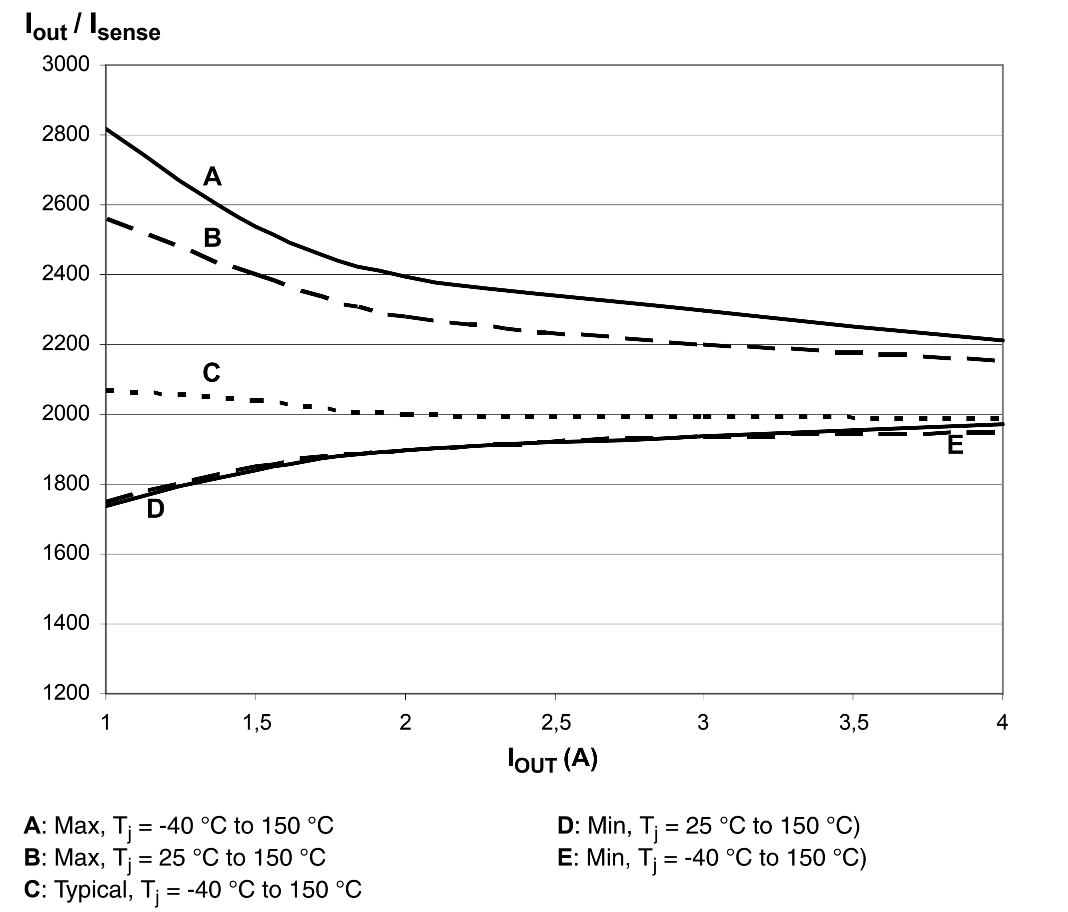
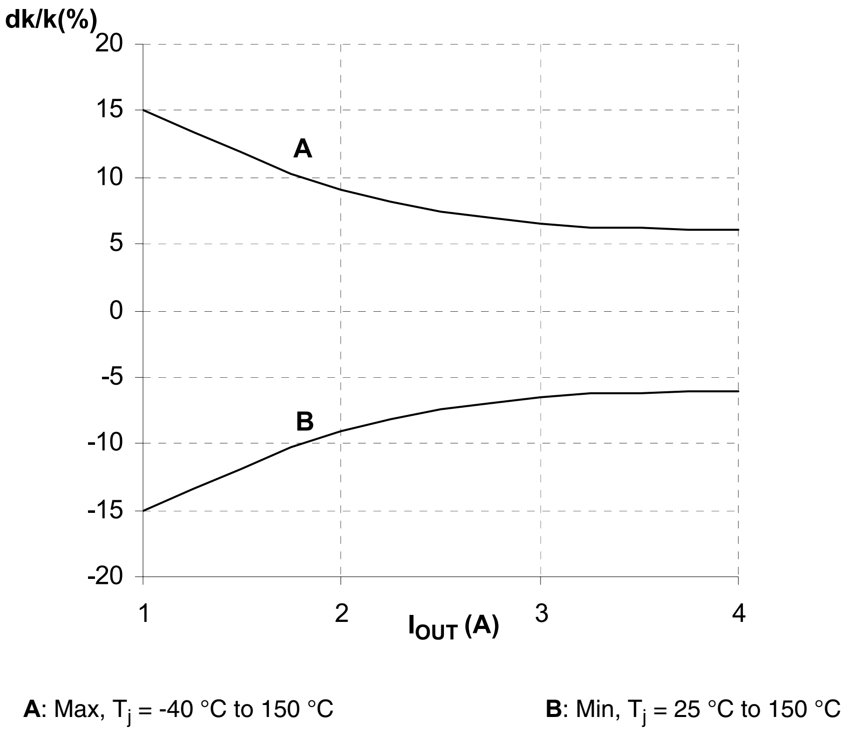


Figure 8. I_{OUT}/I_{SENSE} vs I_{OUT}

Figure 9. Maximum current sense ratio drift vs load current(1)



1. Parameter guaranteed by design; it is not tested.

Table 10. Truth table

Conditions	Input	Output	Sense (V_{CSD} = 0 V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short circuit to GND (power limitation)	L H	L L	0 V_{SENSEH}
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high-impedance, its potential depends on leakage currents and external circuit.

Table 11. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels[1]		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1 h	90 ms	100 ms	0.1µs, 50 Ω
3b	+75 V	+100 V	1 h	90 ms	100 ms	0.1µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b[2]	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 12. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b[1]	C	C

1. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 13. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 10. Normal operation

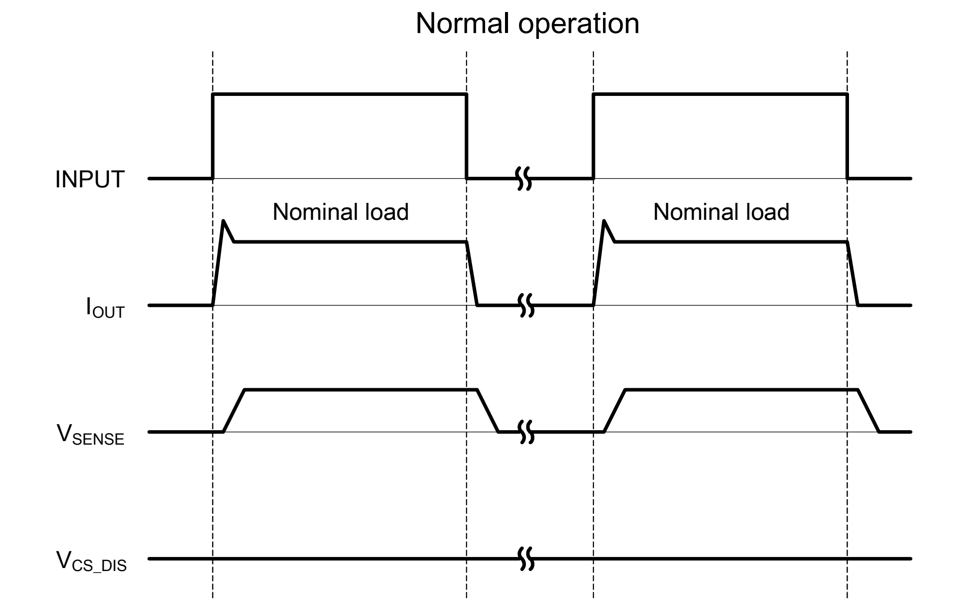


Figure 11. Overload or short to GND

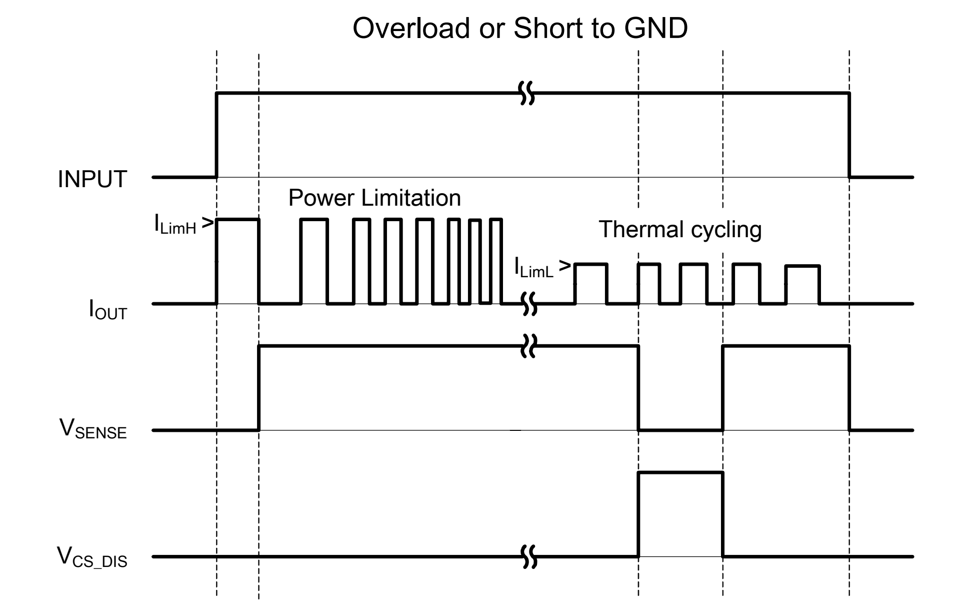


Figure 12. Intermittent overload

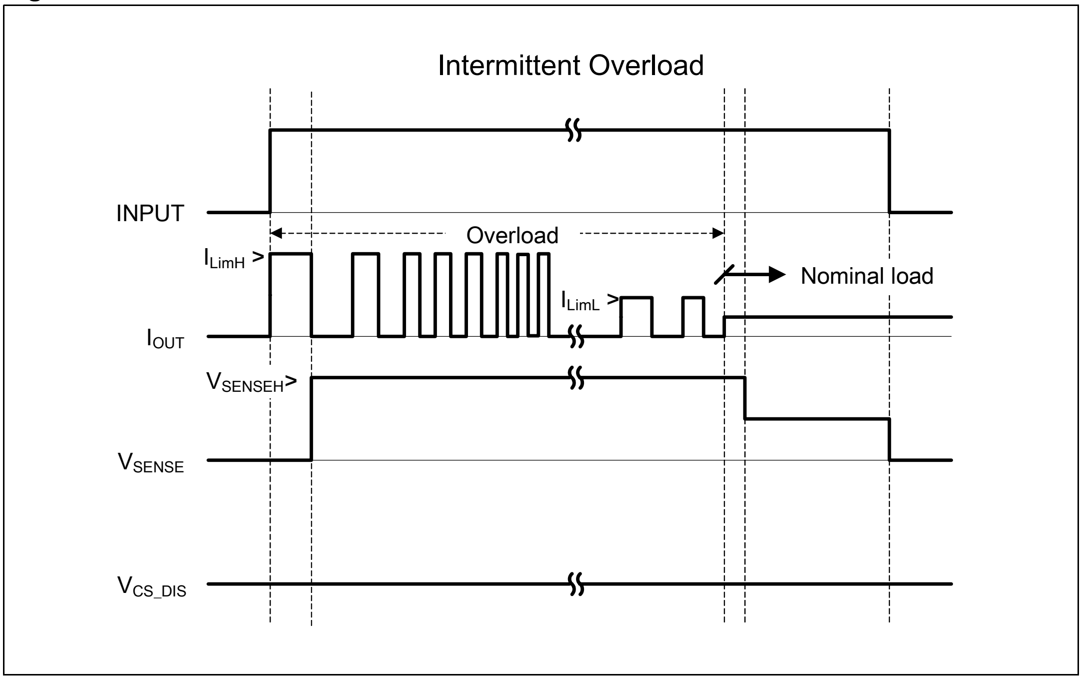
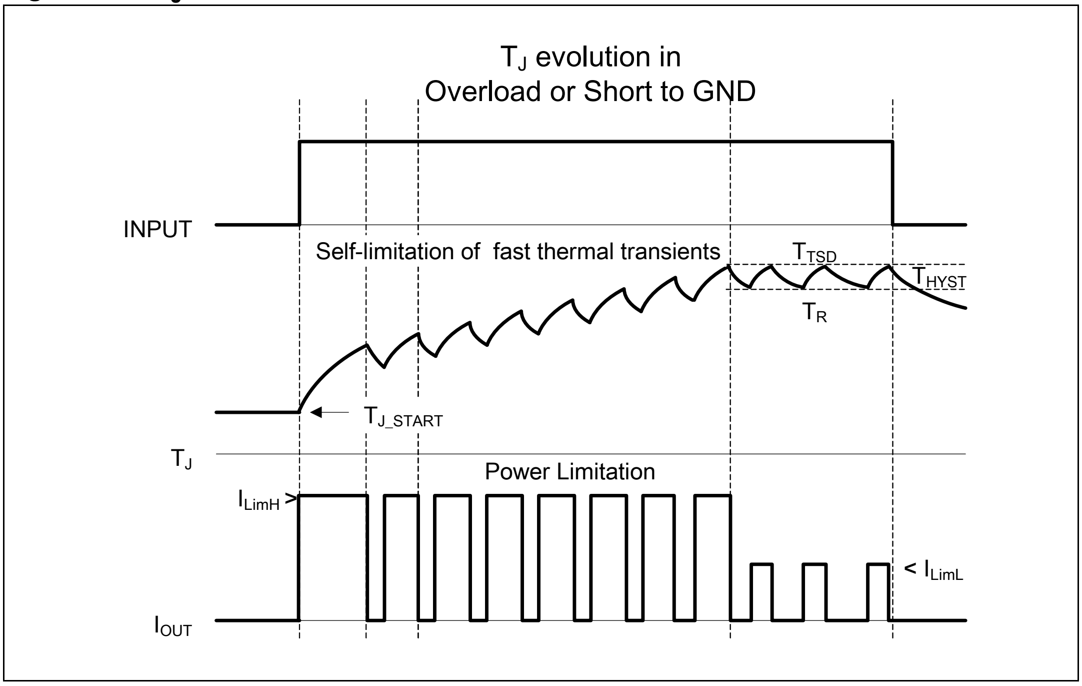


Figure 13. T_J evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 14. OFF-state output current

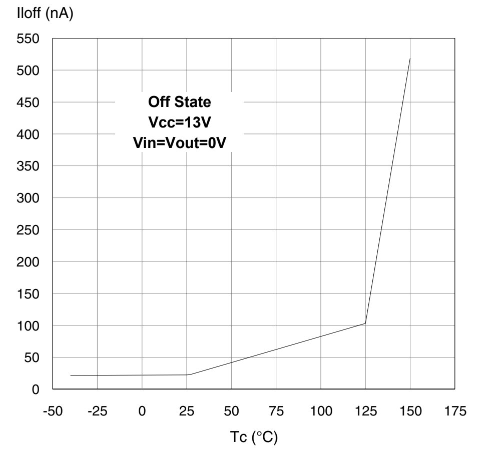


Figure 15. High-level input current

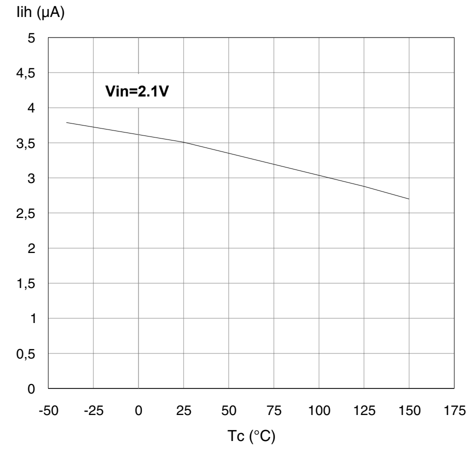


Figure 16. Input voltage clamp

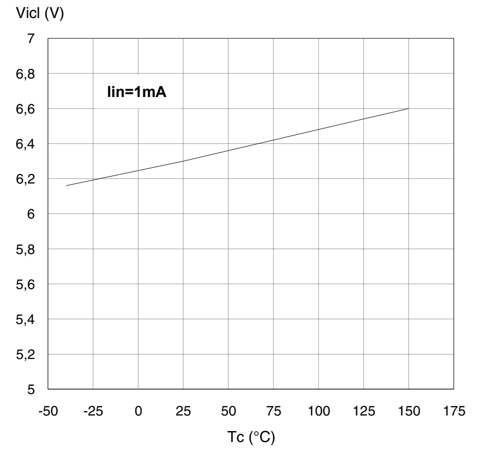


Figure 17. Low-level input voltage

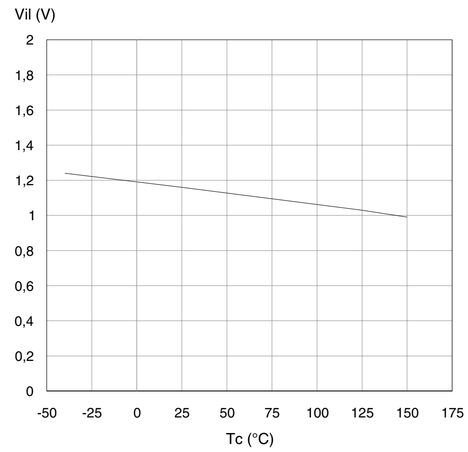


Figure 18. High-level input voltage

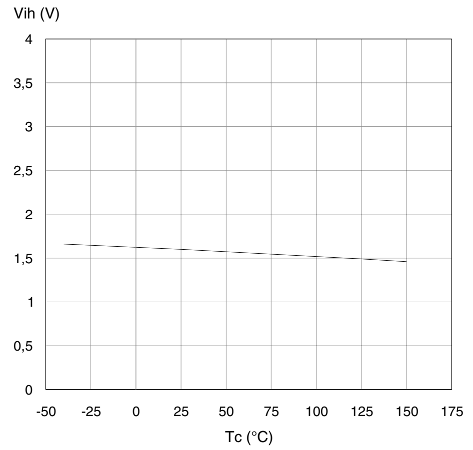


Figure 19. Hysteresis input voltage

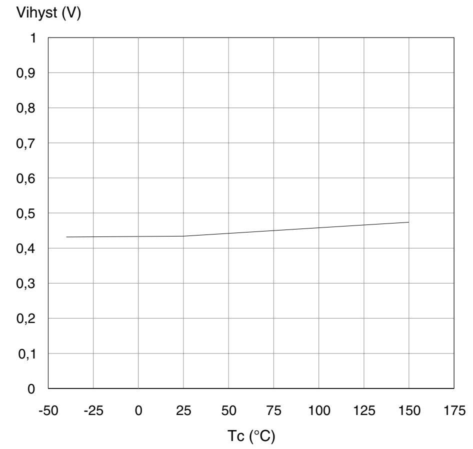


Figure 20. ON-state resistance vs T_{case}

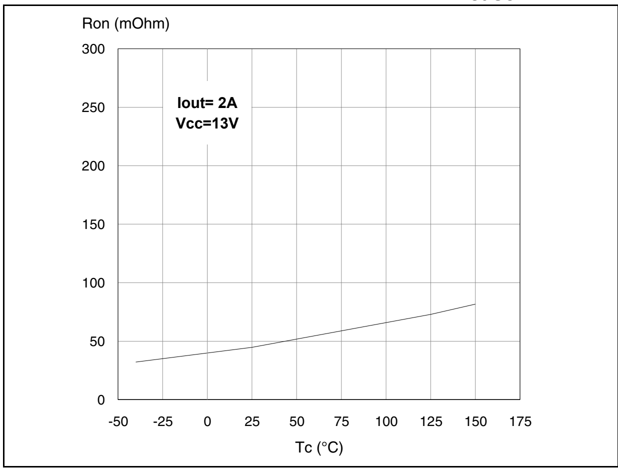


Figure 21. ON-state resistance vs V_{CC}

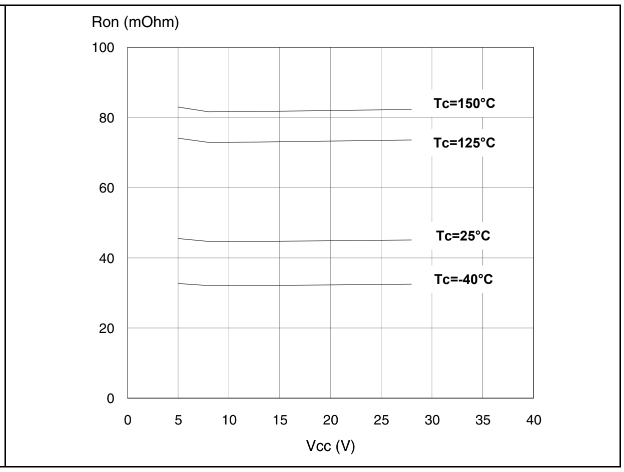


Figure 22. Undervoltage shutdown

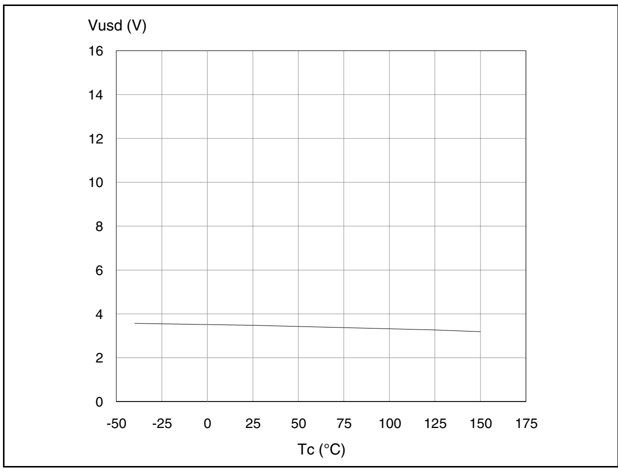


Figure 23. Turn-on voltage slope

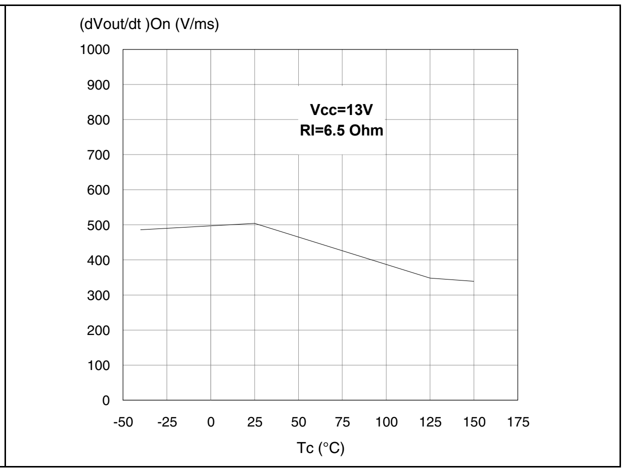


Figure 24. I_{LIMH} vs T_{case}

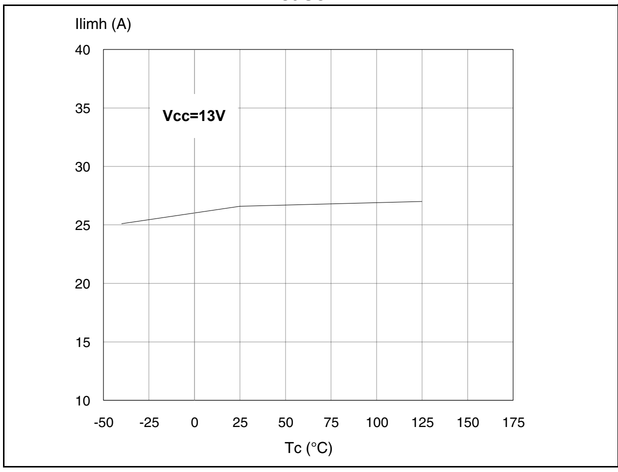


Figure 25. Turn-off voltage slope

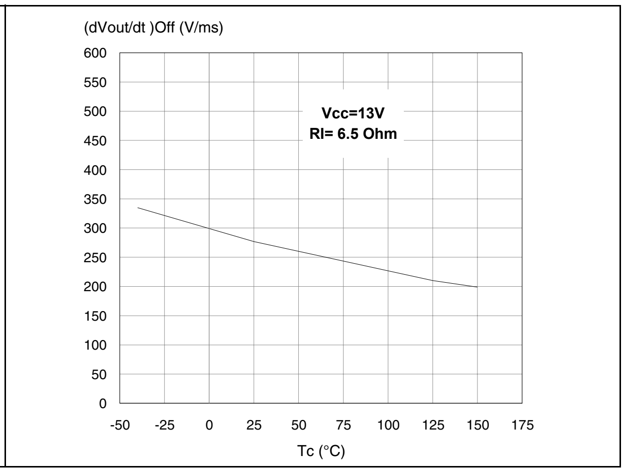


Figure 26. High-level CS_DIS voltage

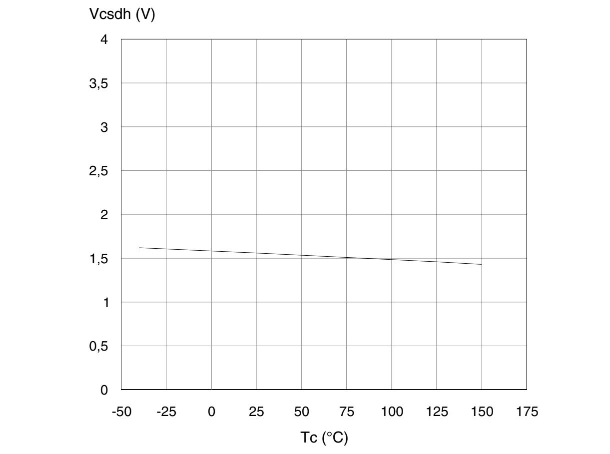


Figure 27. CS_DIS voltage clamp

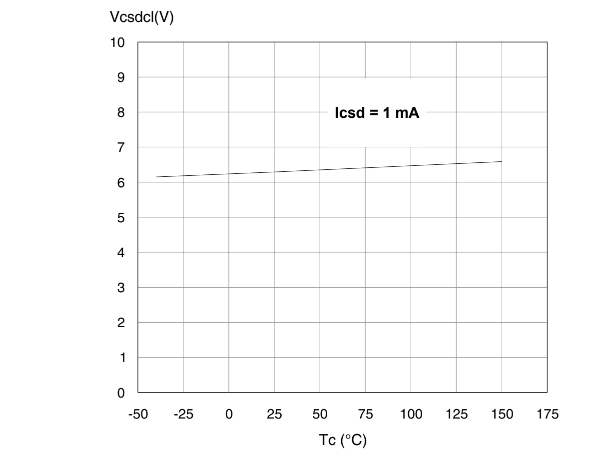
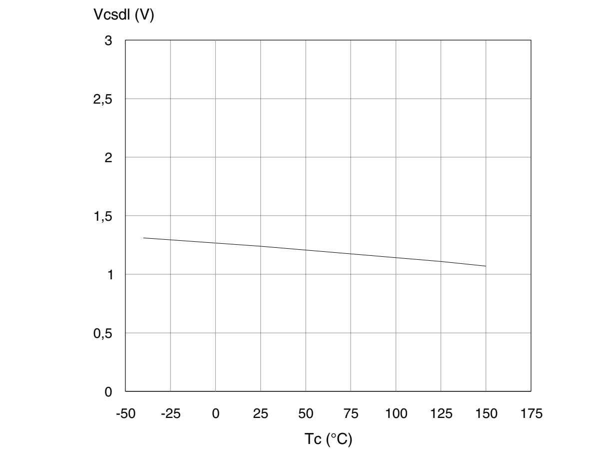
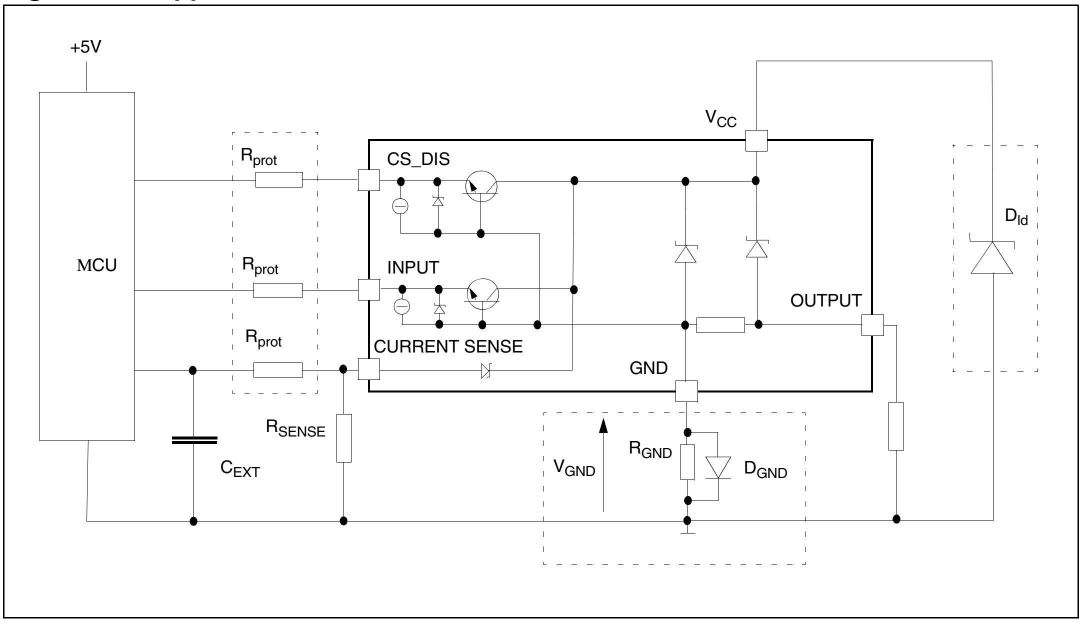


Figure 28. Low-level CS_DIS voltage



3 Application information

Figure 29. Application schematic(1)



1. Channel 2 has the same internal circuit as channel 1.

3.1 GND protection network against reverse battery

This section provides two solutions for implementing a ground protection network against reverse battery.

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1. $R_{GND} \leq 600\ mV / (I_{S(on)max})$
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in R_{GND} (when $V_{CC} < 0$: during reverse battery situations) is:

Equation 1

$$P_D = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} produces a shift ($I_{S(on)max}$ * R_{GND}) in the input thresholds and the status output values. This shift varies depending on how many devices are on in the case of several high-side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see *Section 3.1.2*).

3.1.2 Solution 2: diode (D_{GND}) in the ground line

A resistor (R_{GND} = 1 kΩ) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift not varies if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins is pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os:

Equation 2

$$-V_{CCpeak} / I_{latchup} \le R_{prot} \le (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = - 100 V, $I_{latchup} \ge$ 20 mA and $V_{OH\mu C} \ge$ 4.5 V

5 kΩ ≤ R_{prot} ≤ 180 kΩ

Recommended values: R_{prot} =10 kΩ, C_{EXT} = 10 nF.

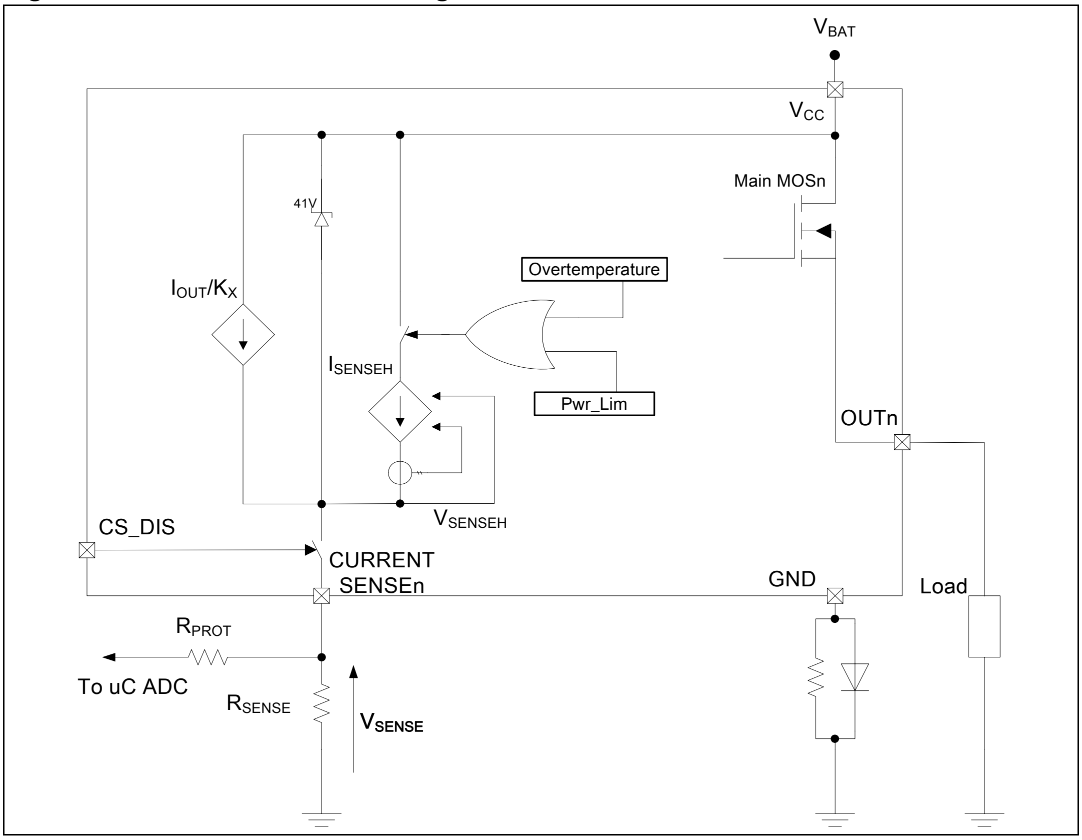
3.4 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 30: Current sense and diagnostic*):

- **Current mirror of the load current in normal operation,** delivering a current proportional to the load one according to a know ratio $\mathbf{K_X}$.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5V minimum (see parameter V_{SENSE} in *Table 9: Current sense (8 V < V_{CC} < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 9: Current sense (8 V < V_{CC} < 18 V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 10: Truth table*):
  - Power limitation activation
  - Over-temperature

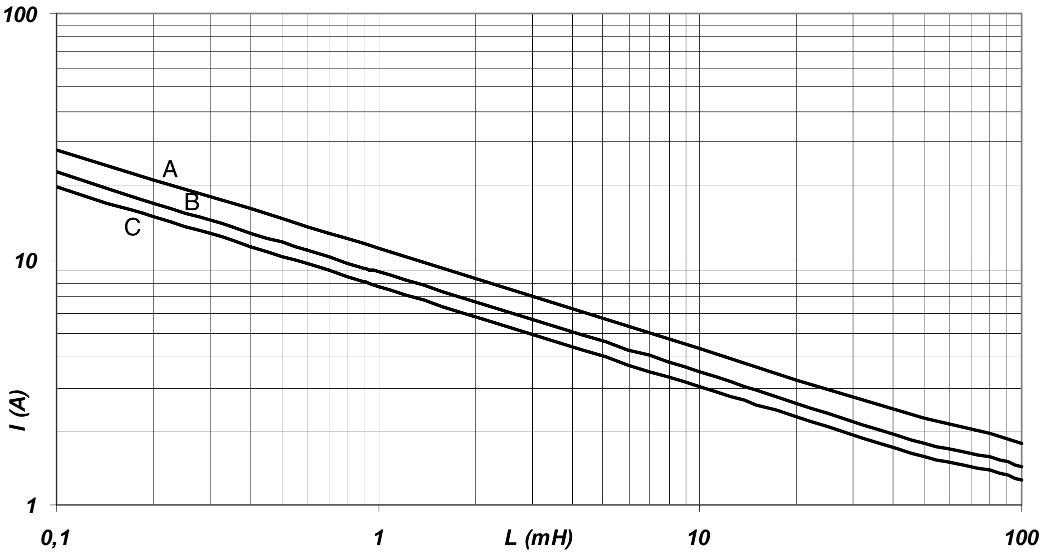
A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high-impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 30. Current sense and diagnostic



3.5 Maximum demagnetization energy (V_{CC} = 13.5 V)

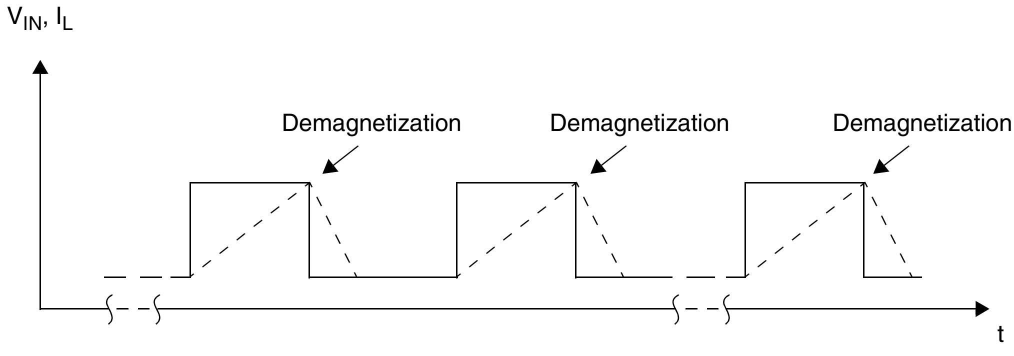
Figure 31. Maximum turn-off current versus inductance (for each channel)(1)



A: T_{jstart} = 150 °C single pulse

B: T_{jstart} = 100 °C repetitive pulse

C: T_{jstart} = 125 °C repetitive pulse

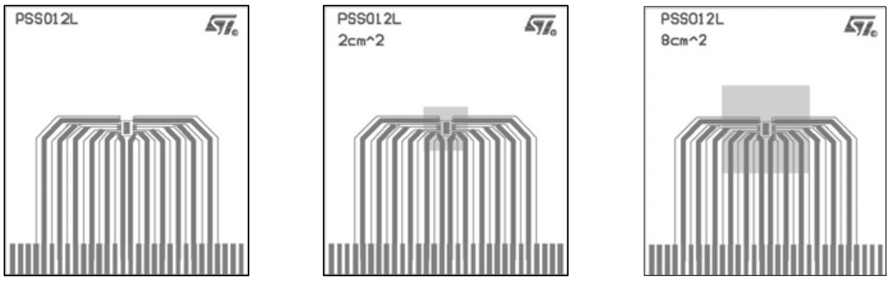


1. Values are generated with R_L = 0 Ω.In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSSO-12 thermal data

Figure 32. PowerSSO-12 PC board(1)



1. Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 µm (front and back side), copper areas: from minimum pad lay-out to 8 cm^2).

Figure 33. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)

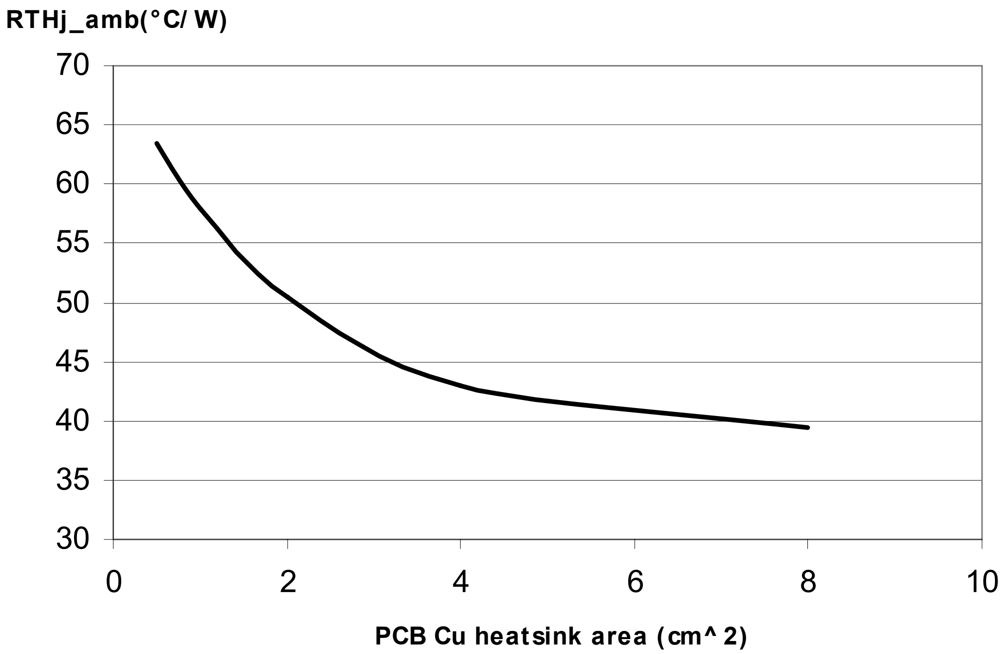
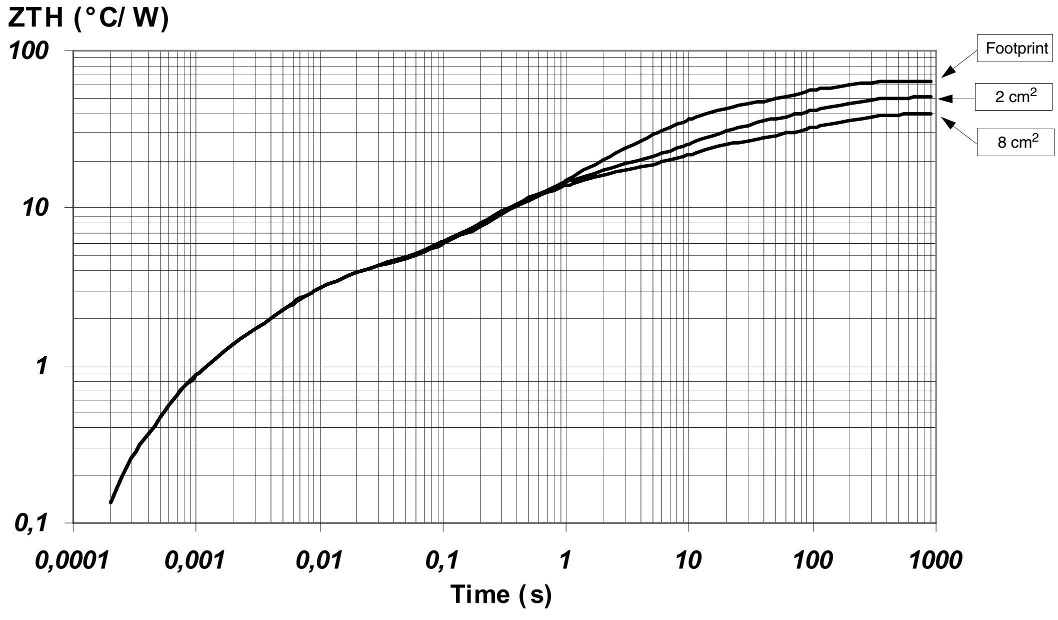


Figure 34. PowerSSO-12 thermal impedance junction ambient single pulse (one channel on)

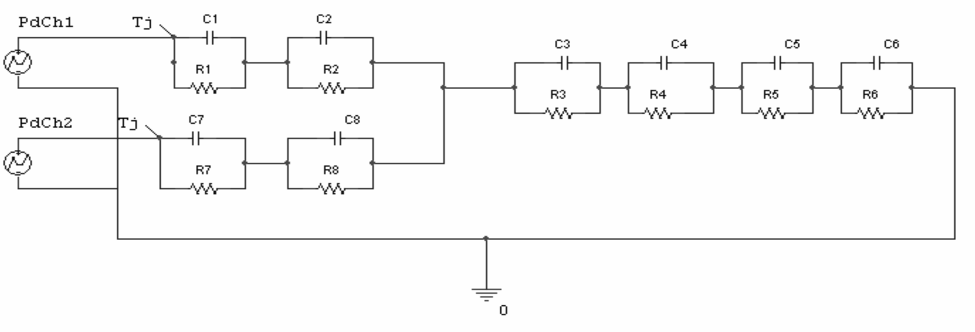


Equation 3: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 35. Thermal fitting model of a double-channel HSD in PowerSSO-12(1)



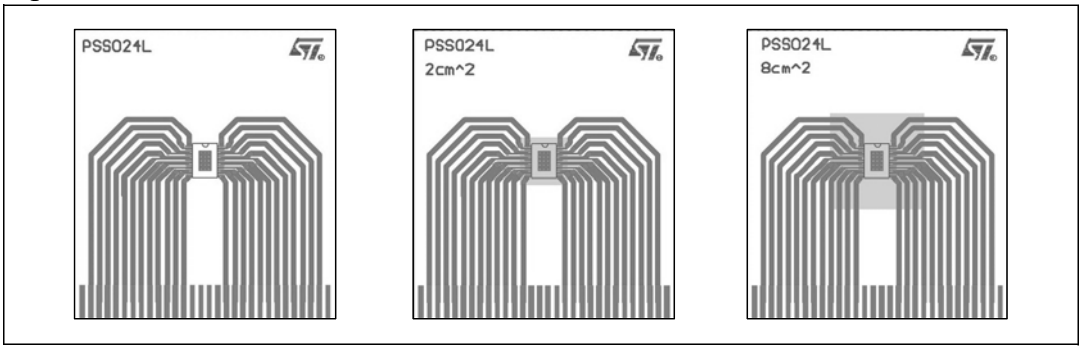
1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 14. Thermal parameters

Area/island (cm^2)	Footprint	2	8
R1=R7 (°C/W)	0.7		
R2=R8 (°C/W)	2.8		
R3 (°C/W)	4		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1=C7 (W.s/°C)	0.001		
C2=C8 (W.s/°C)	0.0025		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

4.2 PowerSSO-24 thermal data

Figure 36. PowerSSO-24 PC board(1)



1. Layout condition of R_{th} and Z_{th} measurements (PCB: double layer, Thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness =1.6 mm, Cu thickness =70 µm (front and back side), Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 37. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)

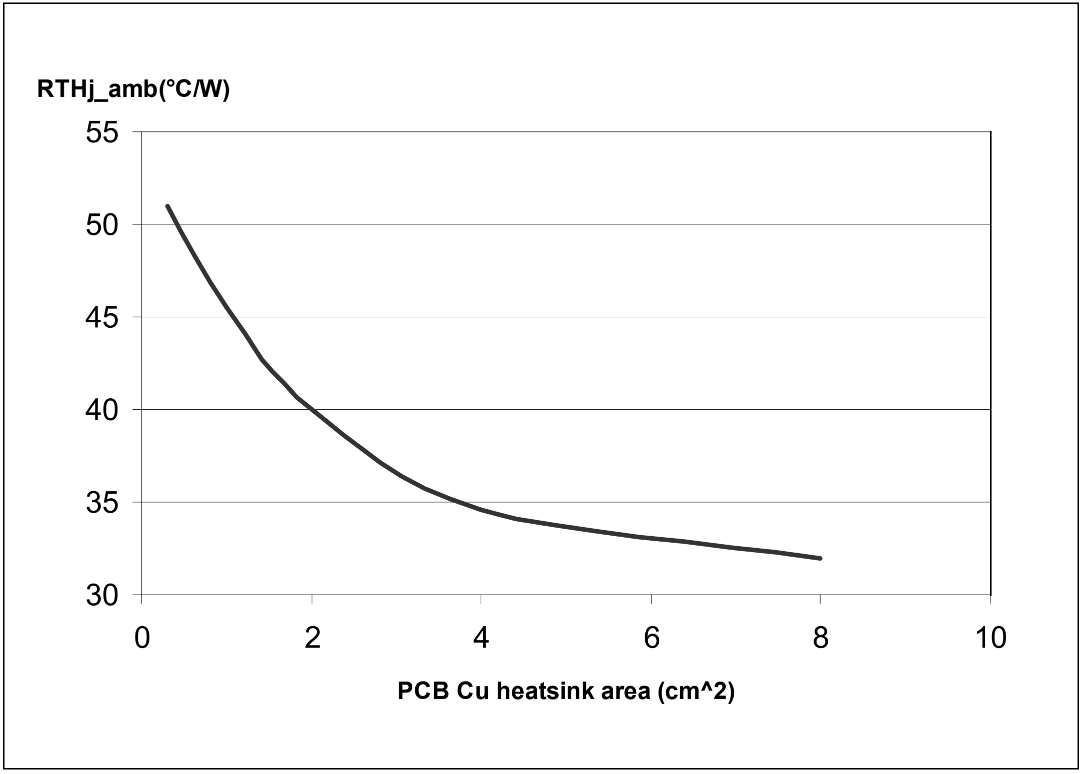
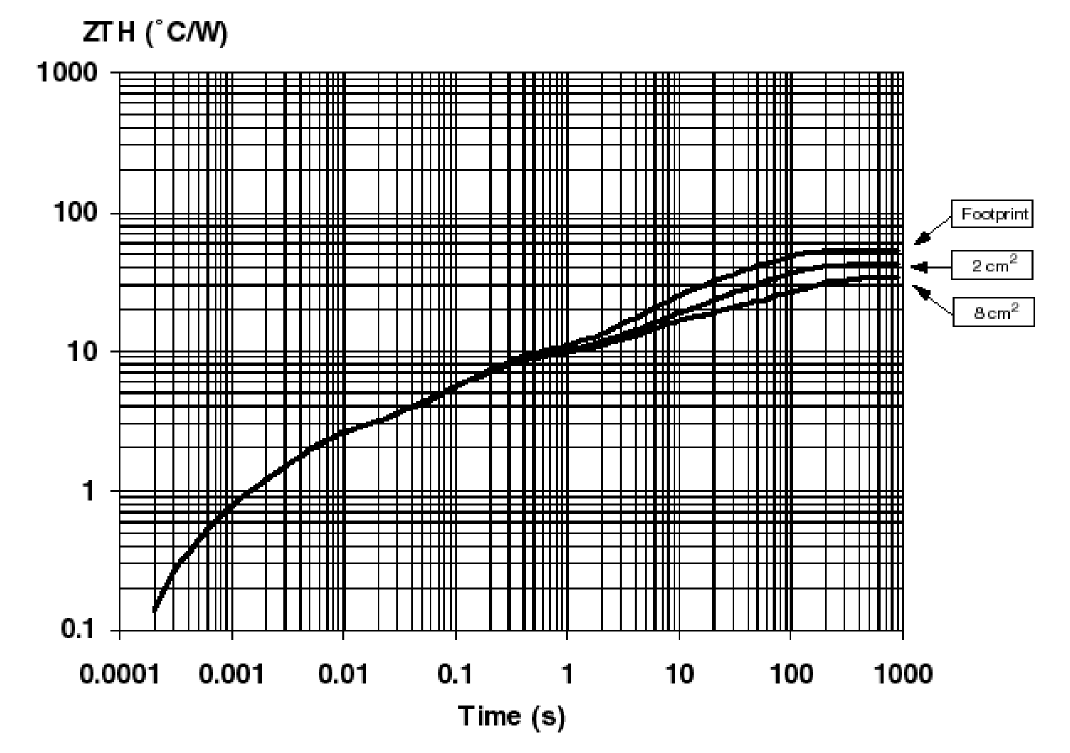


Figure 38. PowerSSO-24 thermal impedance junction ambient single pulse (one channel on)

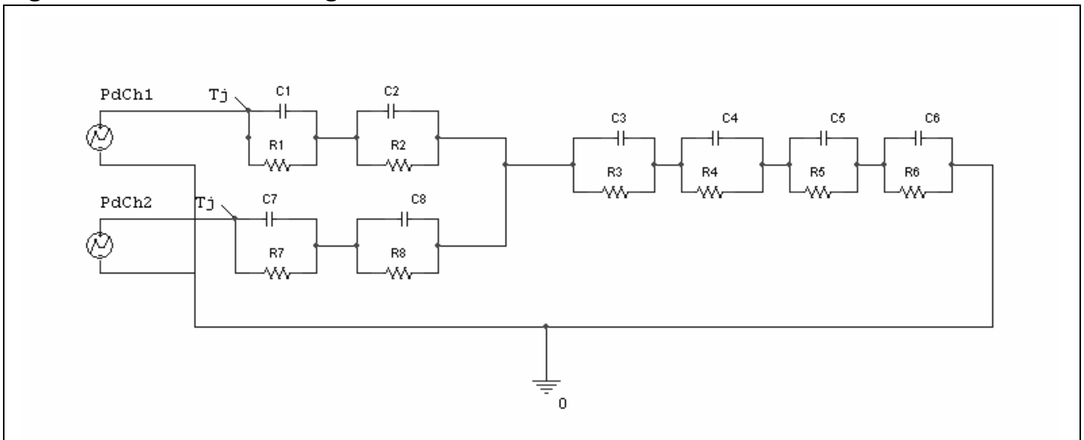


Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Figure 39. Thermal fitting model of a double-channel HSD in PowerSSO-24(1)



1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 15. Thermal parameters

Area / island (cm^2)	Footprint	2	8
R1 = R7 (°C/W)	0.4		
R2 = R8 (°C/W)	2		
R3 (°C/W)	6		
R4 (°C/W)	7.7		
R5 (°C/W)	9	9	8
R6 (°C/W)	28	17	10
C1 = C7 (W.s/°C)	0.001		
C2 = C8 (W.s/°C)	0.0022		
C3 (W.s/°C)	0.025		
C4 (W.s/°C)	0.75		
C5 (W.s/°C)	1	4	9
C6 (W.s/°C)	2.2	5	17

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

5.2 PowerSSO-12 package information

Figure 40. PowerSSO-12 package dimensions

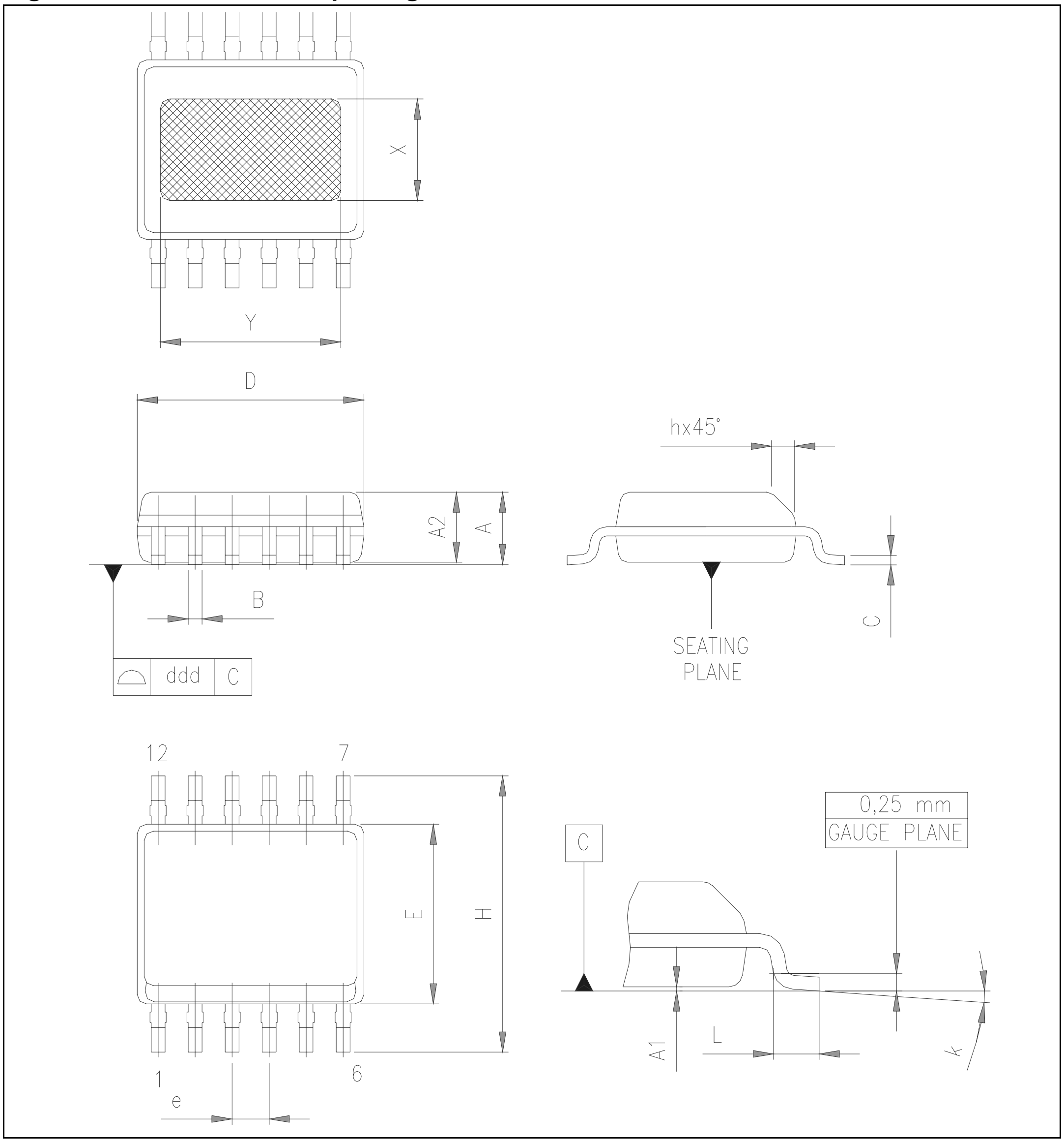


Table 16. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.25		1.62
A1	0		0.1
A2	1.10		1.65
B	0.23		0.41
C	0.19		0.25
D	4.8		5.0
E	3.8		4.0
e		0.8	
H	5.8		6.2
h	0.25		0.5
L	0.4		1.27
k	0°		8°
X	1.9		2.5
Y	3.6		4.2
ddd			0.1

5.3 PowerSSO-24 package information

Figure 41. PowerSSO-24 package dimensions

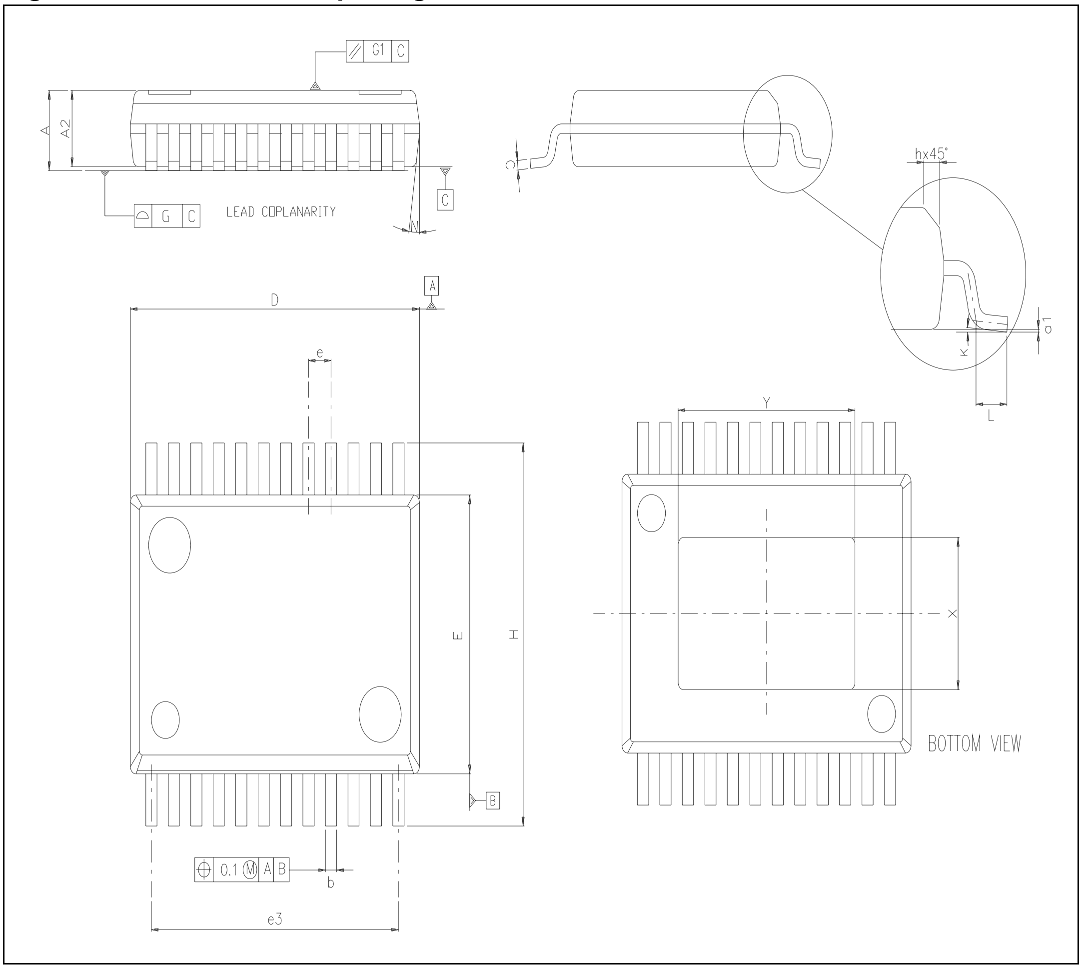
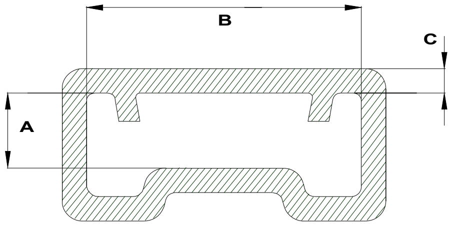


Table 17. PowerSSO-24 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85
N			10deg
X	4.1		4.7
Y	6.5		7.1

5.4 PowerSSO-12 packing information

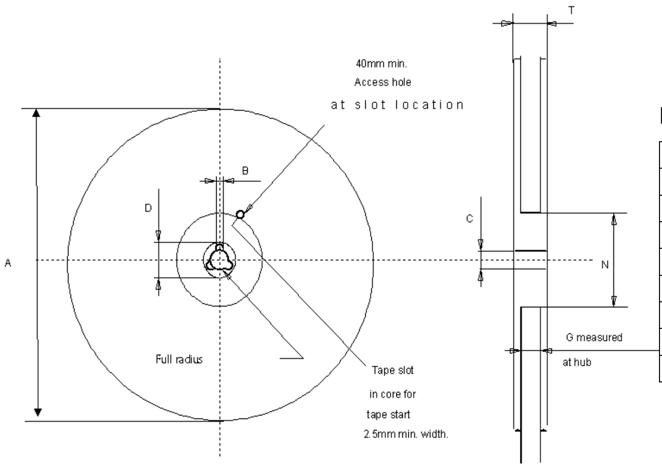
Figure 42. PowerSSO-12 tube shipment (no suffix)



Base q.ty	100
Bulk q.ty	2000
Tube length (± 0.5)	532
A	1.85
B	6.75
C (± 0.1)	0.6

All dimensions are in mm.

Figure 43. PowerSSO-12 tape and reel shipment (suffix “TR”)



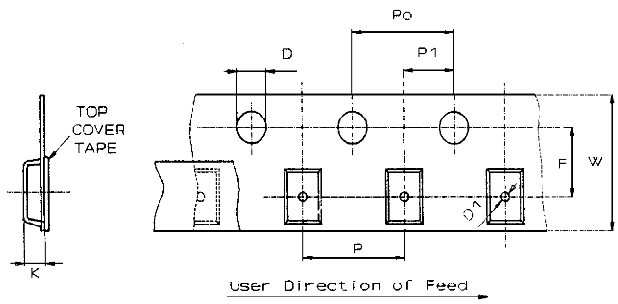
Reel dimensions

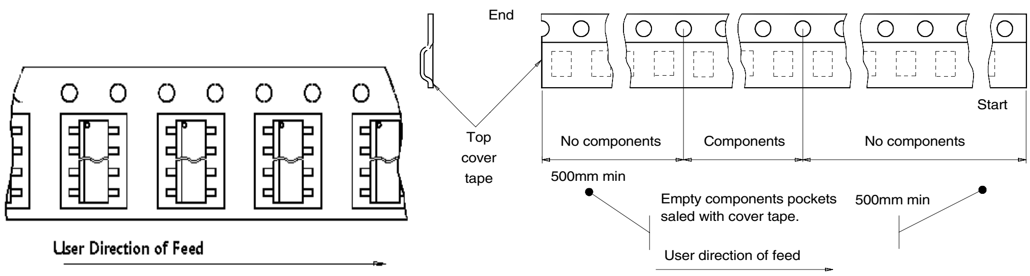
Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

Tape dimensions
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	12
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	8
Hole diameter	D (± 0.05)	1.5
Hole diameter	D1 (min)	1.5
Hole position	F (± 0.1)	5.5
Compartment depth	K (max)	4.5
Hole spacing	P1 (± 0.1)	2

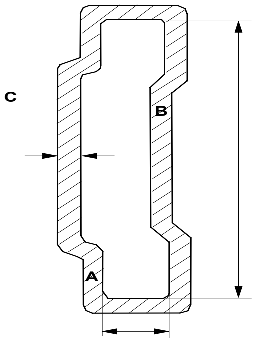
All dimensions are in mm.





5.5 PowerSSO-24 packing information

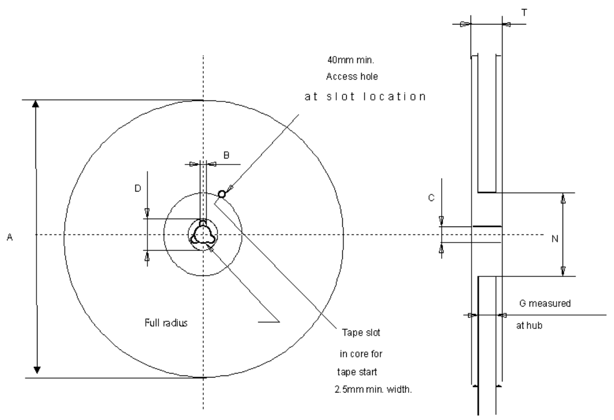
Figure 44. PowerSS0-24 tube shipment (no suffix)



Base qty	49
Bulk qty	1225
Tube length (±0.5)	532
A	3.5
B	13.8
C (±0.1)	0.6

All dimensions are in mm.

Figure 45. PowerSSO-24 tape and reel shipment (suffix “TR”)



Reel dimensions

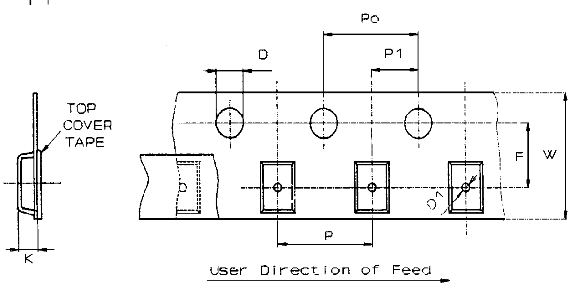
Base qty	1000
Bulk qty	1000
A (max)	330
B (min)	1.5
C (±0.2)	13
F	20.2
G (+2 / -0)	24.4
N (min)	100
T (max)	30.4

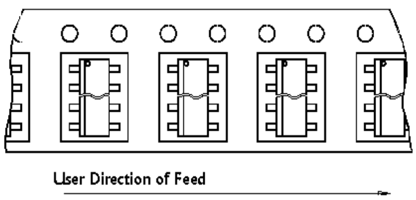
Tape dimensions

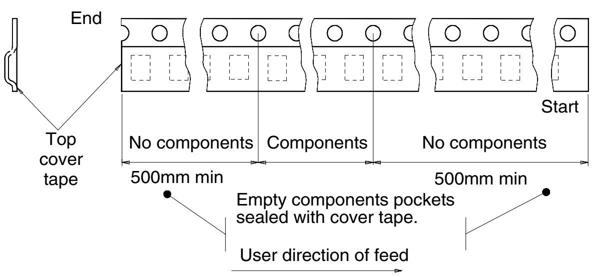
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

Tape width	W	24
Tape hole spacing	P0 (±0.1)	4
Component spacing	P	12
Hole diameter	D (±0.05)	1.55
Hole diameter	D1 (min)	1.5
Hole position	F (±0.1)	11.5
Compartment depth	K (max)	2.85
Hole spacing	P1 (±0.1)	2

All dimensions are in mm.







6 Order codes

Table 18. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSSO-12	VND5E050MJ-E	VND5E050MJTR-E
PowerSSO-24	VND5E050MK-E	VND5E050MKTR-E

7 Revision history

Table 19. Document revision history

Date	Revision	Changes
14-Oct-2009	1	Initial release.